**Bidirectional Buffer with A Non-inverting CMOS input**

**(and gated pull-down and pull-up, and strength 4ma, @3.3V, Normal, High noise(100MHZ), @OSU 180 nm)**

Submitted by N. Gowthami, NIT Rourkela

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***Abstract*—This paper proposes a bidirectional buffer with non-inverting CMOS input, which uses 180nm technology and with specified input voltage and output current.**

# INTRODUCTION

Buffer acts as a non-inverter, whereas CMOS acts like an inverter. CMOS buffer, which is formed by cascading two CMOS inverters, works just like a buffer. 180 nm technology or 0su018 indicates that the channel length in the MOSFET is equal to 180 nanometers. Channel length can be further reduced for efficiencies like reduction in chip area and power consumption, but performance is a key factor that should be taken care of. 4ma,@3.3V means if a VDD of 3V is supplied, we will get an output current of 4ma.

# BIDIRECTIONAL BUFFER

Bidirectional buffer is a logic circuit that amplifies current and power. It consists of two tri-state buffers which are connected in parallel.

BUFFER:

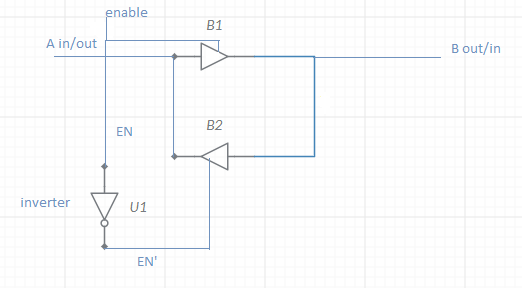
Buffer is a device that has a single input and a single output. Buffer is a non-inverting device. Fan-out of the buffer is very high, which leads to its use to drive high current loads [1]. Buffer has a gain of one.

TRI-STATE BUFFERS:

Tri-state buffer is a buffer with enable input. If enable input is given active high, the circuit works else it doesn’t. High Z is the high impedance state where the output is electrically disconnected, occurs when E=0. When the E=1, it acts like a non-inverting buffer.[3]

BIDIRECTIONAL BUFFER:

It is also called a transreciever circuit as it both transmits and receives the information [4]. We use one active-high and one active low tri-state buffers to achieve this. We add an inverter to the enable input and use it for both. The two tri-state buffers are connected in parallel.



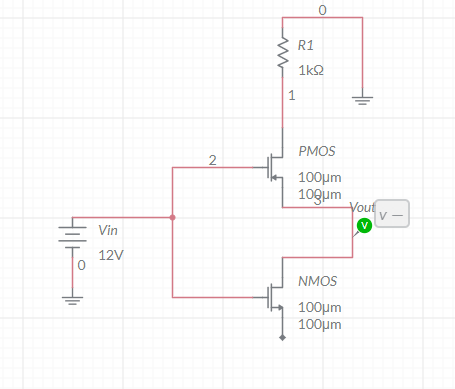
When E=1 data passes from A to B via buffer 1, and when E=0 data pass from B to A via buffer2. Here enable acts as a control to data flow allowing data to flow in either direction.

III. CMOS

CMOS (complementary metal-oxide-semiconductor) is fabricated by using an NMOS pull-down network and a PMOS pull-up network connected in parallel. CMOS technology is used to produce IC’s (Integrated Circuits).

PMOS: p-type metal oxide semiconductor is a MOSFET in which source and drain are p-type, and a body is n-type. In this p-type channel is created by applying a voltage to the gate. In PMOS current flows from source to drain. The output is taken near to the ground. PMOS acts like an inverter, if the input is logic 0, it gets short-circuited, and hence the output is logic one, and when input is logic one, it gets open-circuited, and output is logic 0.[6]

NMOS: n-type metal oxide semiconductor is a type of MOSFET in which source and drain are p-type, and the body is n-type. In NMOS current flows from drain to source. The output is taken near to VDD. NMOS also acts as an inverter. If the input is logic 0 circuit gets open-circuited, and output is logic 1, and when input is logic one, it gets short-circuited, and hence the output is logic 0.[6]

CMOS:

CMOS acts like an inverter. When an input is logic 0 output is logic one and vice-versa. The on and off states of NMOS and PMOS are changed accordingly. CMOS has a high input impedance, high noise immunity, and low power consumption [5].

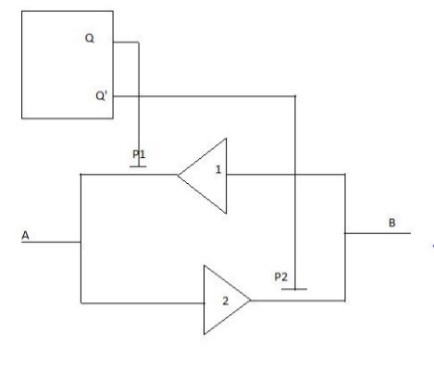
IV APPLICATIONS:

In the IC industry, circuits whose performance can be taken place in the smallest possible area and at the greatest amount of speed are required.

1. BIDIRECTIONAL BUFFER AMPLIFIER:

It has two control signals, namely Q and Q’ which are complementary to each other. The circuit includes two pass transistors or CMOS transmission gates, each of which are controlled by the control signals Q and Q’ respectively. A pass transistor is a transistor that either transmits or blocks a signal received. There are two leads, one of which acts as an input the other as an output. For a particular selection of Q and Q,’ the bi-directional amplifier receives an input signal on the first lead and produces an amplified output signal on the second lead. For the second option of Q and Q’, the input is received on the second lead, and an amplified output is given through the first lead. [8]

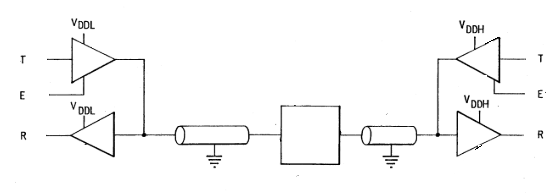
The circuit contains two transistors, the first one is for passing a first input signal on first terminal to input lead or passing output signal on output lead to first terminal. The second one selectively passes second input signal on second terminal to input lead or output signal on output lead to second terminal.



1. BIDIRECTIONAL LEVEL SHIFTING INTERFACE CIRCUIT

It has first and second I/O ports that are connected by a drain-source channel FET that passes signals between them in both the directions. The first port is connected to a low supply voltage and the second one to a high supply voltage. This circuit also contains an inverter having a control input connected to the second port. The control input of the latching FET is connected to an inverted output so that when the second port exhibits logic one, the inverted output becomes logic 0 and activates the p channel FET to drive the second circuit at logic one.[9]

This level shifting interface circuit is used between two circuits operating at different voltages. The interface circuit includes a latching circuit biased with a high voltage. The latching circuit consists of a P channel FET, and the interface circuit consists inverter circuit having control input connected to the second port. The gate of P channel FET is connected to the inverted output.



1. GPIO (general purpose input /output)

GPIO has no predefined function. It is customizable and is controlled by the user. It has an enable which selects the input or output buffer. If enable=0 output buffer gets 1 and it gets activated in output mode. If enable=1 pin gets activated in input mode [12]. Ouput buffer is a combination of two cmos transistors connected in the following fahion. Input buffer is the reverse of output buffer which means output from the pin is inverted and fed to the drains of both pmos and nmos. By default all GPIO pins are configured in input mode. In input mode pin is kept floating that is it is neither connected to VCC nor GND, this state is called high impedance state it may cause high power consumption due to leakage current.when pin is not floating it may be either connected to VCC or GND in both the cases there is no leakage current from VCC to GND. [11]

Default state for output mode is push-pull. It uses both pmos and nmos in its configuration. An LED is connected to the pin along with a current limiting resistor. If input is 1 LED is on and viceversa.

Open drain configuration:

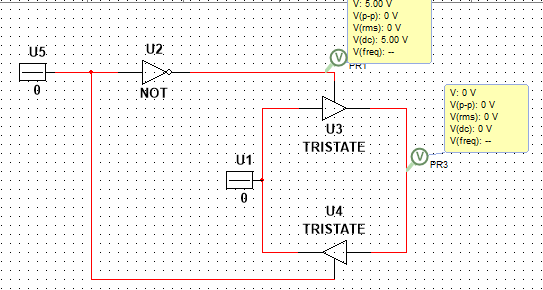
Only NMOS trasnsistor is active, we can neglect the presence of PMOS. If input is 0 output is pulled to ground, if input is 1 output is floating this implies open drain can cause two states GND and floating to make use of this configuration we need to provide pull up capability. This can be done in two ways internal and external pull-up resistors. Pin is pulled up to VCC if input is 1 in this case LED will be turned ON.

V. IMPLEMENTATION OF GPIO

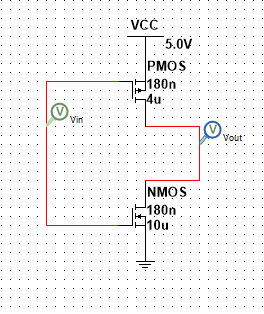
PMOS and NMOS with fixed length (180nm) snd varying widths are taken. Vary the widths such that (W/L)p is 2 to 3 times of (W/L)n for switching threshold to be optimum.

As l=180nm for both NMOS and PMOS we can take Wp=4um, and Wn=10um that gives (W/L)p=22.5, and (W/L)n=55.5 which is 2.5 times of (W/L)p [13]

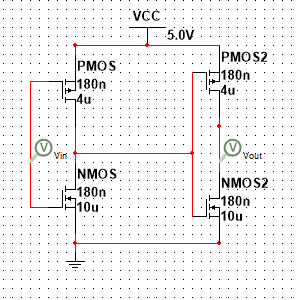
Bidirectional buffer circuit:

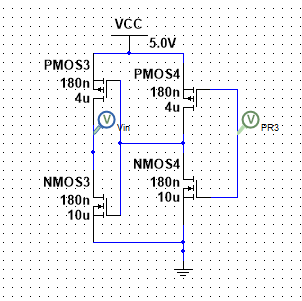
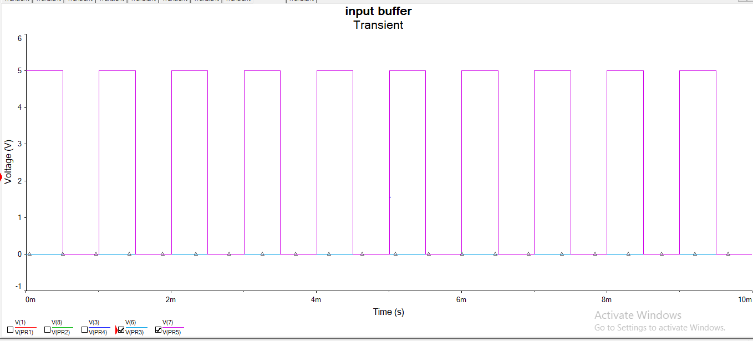


The following is a basic CMOS inverter circuit:

A buffer circuit formed by using an inveter and CMOS inverter or by combining two CMOS. If the input is given logic 1, output is also logic 1 and if the input is logic 0 output is also logic 0. This shows that it acts like a buffer that does not change the state of input .

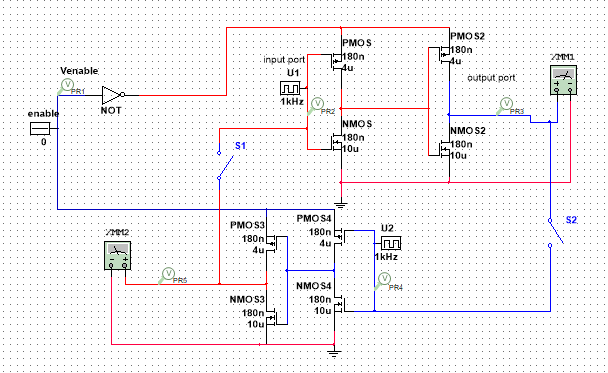
The following is a output buffer circuit:





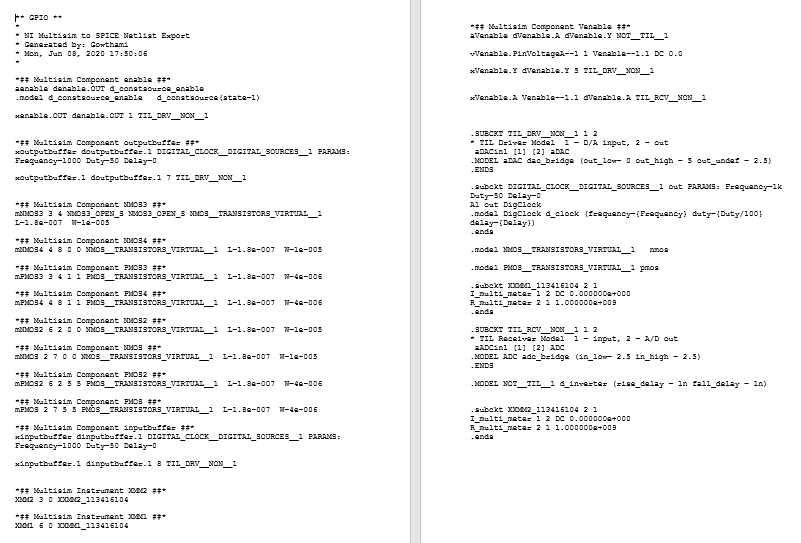
The circuit of input buffer iIt is the exact opposite of the output buffer

GPIO CIRCUIT

If the enable input is logic 1(high) output buffer gets logic 0(low) and input buffer gets logic 1(high) and pin gets activated in input mode. If the enable input is logic 0(low) output buffer gets logic 1(high) and input buffer gets logic 0(low) and pin gets activated in output mode. Hence if the enable is high input mode is selected and viceversa. When the output buffer is activated with the enable 0 PR2 is a clock input given which gives the same clock output passing through the buffer and simultaneously the input buffer is deactivated and its output is zero voltage. When input buffer is activated with enable 1

SPICE NETLIST:

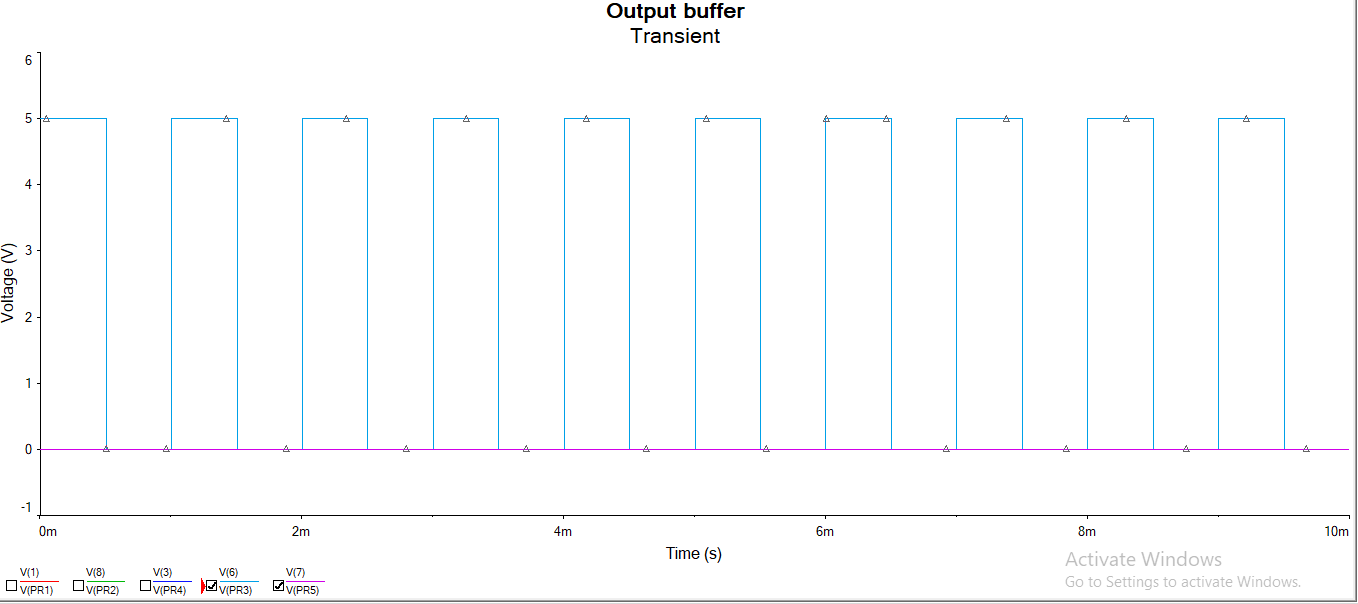
It is a text form of representing a circuit. It can help in finding simulation errors



OUTPUT GRAPHS:

Input mode is selected when the enable is given active high hence the output of input buffer is the same as its input, a clock pulse. While the output of output buffer is zero as it does not work.

Output mode is selected when the enable is given active low and hence the output of output buffer is same as its input, a clock pulse. While the output of input buffer is zero as it does not work.



# REFERENCES

1. <http://users.etown.edu/w/wunderjt/333_BUFFERS.pdf>.
2. <https://en.wikipedia.org/wiki/Digital_buffer>.
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